CBCS SCHEME

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17EC53

Fifth Semester B.E. Degree Examination, Aug./Sept.2020
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the typical design flow with verilog HDL for designing VLSI IC. **(10 Marks)**
b. What is Instance and Instantiation? Explain with suitable example. **(10 Marks)**

OR

2 a. Taking D_FF as an instance, write a verilog code for D-Flip flop for Synchronous Reset. **(05 Marks)**
b. Compare top-down and bottom-up design methodology. **(07 Marks)**
c. Explain design hierarchy using 4-bit ripple carry counter. **(08 Marks)**

Module-2

3 a. Explain the lexical convention “X/Z values”. **(02 Marks)**
b. Explain how ports are connected to external signals. **(08 Marks)**
c. Define the following data type with example :
(i) Nets (ii) Registers (iii) Vectors (iv) Array (v) Parameter. **(10 Marks)**

OR

4 a. Explain the usage of ′define and ′include compiler directives. **(05 Marks)**
b. With a generalized example, explain the components of verilog module. **(07 Marks)**
c. Write a verilog code to implement the sequential circuit shown below in Fig.Q4(c). Write stimulus for the same.

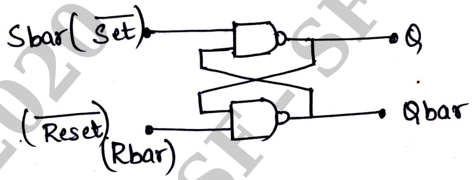

Fig.Q4(c) **(08 Marks)**

Module-3

5 a. Design a gate level module according to the logic diagram given in Fig.Q5(a). Write stimulus.

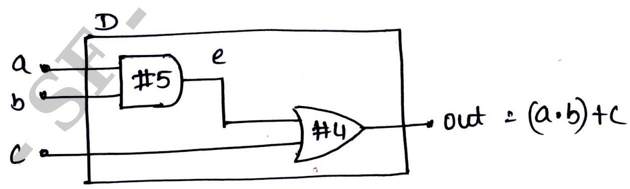

Fig.Q5(a) **(05 Marks)**
b. Define the terms: Rise, Fall and Turn off delays. **(05 Marks)**
c. Write the block diagram, gate level logic diagram of a 4:1 multiplexer. Write a verilog code for the same using gate level logic description. Write stimulus. **(10 Marks)**

OR

6 a. What are the output for the following instructions:
(i) Y = 1X ; X = 4′b1010
(ii) Y = X << 1 ; X = 4′b0101
(iii) Y = {B, C, 2′b11}; B = 4′b0010 , C = 4′b1101
(iv) Y = {4{A}, 3{B}}; A = 1′b1, B = 2′b01
(v) Y = A + B ; A = 4′b1010, B = 4′b1110 **(05 Marks)**

b. Write the truth table for all Bitwise operator. **(05 Marks)**

c. Develop a gate level verilog code for 4-bit ripple carry adder from 1-bit full adder. What is the out if A = 0110 B = 1110 and C_{in} = 0 at t = 0 **(10 Marks)**

Module-4

7 a. Explain how the initial and always statements are declared and used in verilog code. **(10 Marks)**

b. Explain Non blocking statement. Mention one application example. **(10 Marks)**

OR

8 a. With an example and formal syntax definition. Explain conditional 'if' 'else' statements. **(05 Marks)**

b. Design a 4:2 priority encoder with i_3, i_2, i_1 and i_0 as inputs and y_1 y_0 are outputs. If i_3 is 1 output shall be 11, i_2 is 1 output shall be 10, i_1 is 1 output shall be 01 and i_0 is 1 output shall be 00; by default let output be 00 **(05 Marks)**

c. Explain the following loops with example:
(i) FOR LOOP (ii) FOREVER LOOP (iii) WHILE LOOP **(10 Marks)**

Module-5

9 a. Write a VHDL code to implement 4-bit equality comparator using Behavioral description. **(04 Marks)**

b. Explain the integer type, physical type and array data types in VHDL. **(06 Marks)**

c. With a neat tool flow diagram, explain design tool flow. **(10 Marks)**

OR

10 a. Explain the following modes of ports :
(i) IN (ii) OUT (iii) BUFFER (iv) INPUT. **(08 Marks)**

b. Explain what are signals and constants. How are they declared and used in VHDL code? **(05 Marks)**

c. Write a short note on Attributes in VHDL. **(07 Marks)**

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